ESE 585 Nanoscale Integrated Circuit Design **Spring 2019**

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Office: Room 257, Light Engineering Building
Office hours: Wednesdays 9:30 am to 11:30 am and Thursdays 11 am to 1 pm

Course Description:

This course describes high performance and low power integrated circuit (IC) design issues for advanced nanoscale technologies. After a brief review of VLSI design methodologies and current IC trends, fundamental challenges related to the conventional CMOS technologies are described. The shift from logic-centric to interconnect-centric design is emphasized. Primary aspects of an interconnect-centric design flow are described in four phases: (1) general characteristics of on-chip interconnects, (2) on-chip interconnects for data signals, (3) on-chip power generation and distribution, and (4) on-chip clock generation and distribution. Existing design challenges faced by IC industry are investigated for each phase. Tradeoffs among various design criteria such as speed-power-noise-area are highlighted. In the last phase of the course, several post-CMOS devices, emerging circuit styles, and architectures are briefly discussed. At the end of the course, the students will have a thorough understanding of the primary circuit and physical level design challenges with application to industrial IC design.

Prerequisite: Graduate students: ESE 555, Undergraduate students: ESE 330 and ESE 355.

Teaching Material:

Required

Book

- E. Salman and E. G. Friedman, *High Performance Integrated Circuit Design*, McGraw-Hill, 2012.

Reviews and tutorial papers on related subjects distributed during class

Recommended

- A. Chandrakasan, W. J. Bowhill, and F. Fox (Editors), *Design of High-Performance Microprocessor Circuits*, Wiley-IEEE Press, 2001..
- L. Scheffer, L. Lavagno, and G. Martin (Editors), *EDA for IC Implementation, Circuit Design, and Process Technology,* CRC Press, 2006.
- Jeffrey A. Davis, James D. Meindl (Editors), *Interconnect Technology and Design for Gigascale Integration*, Kluwer, 2003

Course Content: Course consists of the following four primary parts

- **Introduction**
  - Integrated circuit design process and history
  - Review of MOS transistor theory
  - Device and interconnect scaling
  - Interconnect-centric design
- **On-chip Interconnects**
  - Modeling and extraction
  - Signal propagation and delay analysis
  - Interconnect coupling noise: Crosstalk
  - Substrate coupling noise
  - Global signaling methodologies
- **On-chip Power Networks**
  - Power generation
  - Power and ground distribution
  - Power consumption
  - Low power design techniques
- **On-chip Clock Networks**
  - Synchronization
  - On-chip clock generation
  - Clock distribution
  - Timing optimization of synchronous systems

Grading

- Midterm: 30 %
- Lab assignments: 30%
- Final project and a four page report written in *IEEE* format: 40%

Student Learning Objectives:

- An ability to identify, formulate, and solve engineering problems
- An ability to understand current research issues
- An ability to communicate effectively

Disability Support Services (DSS) Statement:

If you have a physical, psychological, medical or learning disability that may impact your course work, please contact Disability Support Services, ECC (Educational Communications Center) Building, room 128, (631) 632-6748. They will determine with you what accommodations, if any, are necessary and appropriate. All information and documentation is confidential. Students who require assistance during emergency evacuation are encouraged to discuss their needs with their professors and Disability Support Services. For procedures and information go to the following website: http://www.stonybrook.edu/ehs/fire/disabilities.

Academic Integrity Statement:

Each student must pursue his or her academic goals honestly and be personally accountable for all submitted work. Representing another person's work as your own is always wrong. Faculty are required to report any suspected instances of academic dishonesty to the Academic Judiciary. Faculty in the Health Sciences Center (School of Health Technology & Management, Nursing, Social Welfare, Dental Medicine) and School of Medicine are required to follow their school-specific procedures. For more comprehensive information on academic integrity, including categories of academic dishonesty, please refer to the academic judiciary website at http://www.stonybrook.edu/commcms/academic_integrity/index.html

Critical Incident Management Statement:

Stony Brook University expects students to respect the rights, privileges, and property of other people. Faculty are required to report to the Office of Judicial Affairs any disruptive behavior that interrupts their ability to teach, compromises the safety of the learning environment, or inhibits students' ability to learn. Faculty in the HSC Schools and the School of Medicine are required to follow their school-specific procedures.