Spring 2019

ESE 218: Digital Systems Design

Instructor: Dmitri Donetski
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Office Hours: Tuesday, Thursday, 3-5 PM, room 247 Light Eng. bldg.

Prerequisites: Engineering Major: PHY 127 or 132 or 142, or ESE 124; Computer Science Major: CSE 220

Description: The course covers binary numbers, Boolean algebra, arithmetic circuits, flip-flops, analysis and design of sequential circuits, memory and programmable logic. Circuits are designed and simulated in Active-HDL (Aldec), assembled on a breadboard and verified/debugged with a pattern generator/logic analyzer.

Goal: Learning basic theory and development of practical skills for taking next level ECE courses.

Outcomes: students will develop 1) understanding fundamentals of analysis and design of standard building blocks and systems; 2) skills in reading schematic of digital circuits and analysis of circuit behavior; 3) skills in design of combination and sequential circuits using conventional methods and CAD tools; 4) skills in verification and troubleshooting circuits with the pattern generator and logic analyzers, determination of signal propagation delays.

Lectures: 103 Javits, Tuesday, Thursday, 5:30-6:50 PM

Labs: Room 235 Heavy Eng. bldg (new addition). Lab attendance (experiments) starts the week of Feb 11.
Section 1, Monday, 8:55-11:55PM
Section 4, Monday, 12:45-3:45 PM
Section 2, Monday, 7:00-10:00 PM
Section 3, Tuesday, 7:00-10:00 PM

Requirements: 1) Textbook: M. Morris Mano, Michael D. Ciletti, "Digital Design", Pearson, 6th or 5th edition. 6th ed: 2017, ISBN-13: 978-0470531082, ISBN-10: 0470531088, 5th ed.: 2013, ISBN-13: 978-0-13-277420-8, ISBN10: 013-277420-8. All homeworks, prelab and lab assignments with instructions will be posted on the Blackboard.

2) Laptop operating under Windows for circuit design and simulation (prelab assignments).

Prelab reports: Prelab report for simulation part is an individual effort. The prelab reports have to be submitted by email to the instructor by 11:59PM the day before the lab session: Sunday for sections 1, 2, 4, Monday for section 3.

Lab reports: Experiments are completed by a team of two students. The printed final lab reports with the prelab reports of two team members and the report for the experimental effort are collected at the next week lab session.

Grading: Lab reports (40 %), Homeworks (10 %), Test 1 (10 %), Test 2 (15 %), Final exam (25 %). Tentatively grades are assigned as follows: A: > 92, A-: 91-85, B+: 84-78, B: 77-71: B-: 70-64, C+: 63-57, C: 56-50 pts.

Passing the course with grades in A-C range requires: 1) submission of 11 individual prelab reports (simulations) to the instructor; 2) best effort in 11 lab experiments and submission of all final lab reports; 3) understanding of major concepts, ability to design finite state machines demonstrated on tests and the final exam.

Topical outline:

1. Binary numbers and codes: 5 %
2. Boolean algebra, logic transformation and minimization: 20 %
3. Arithmetic circuits, decoders, multiplexers, latches and flip-flops: 25 %
4. Analysis and design of sequential circuits: 40 %
5. Memory and programmable logic: 10 %

Additional reading:

1. F. Vahid, Digital Design with RTL Design, VHDL, and Verilog, 2nd ed, 2010, ISBN-13: 978-0470531082, ISBN-10: 0470531088; 2. D.M. Harris, S.L. Harris, Digital Design and Computer Architecture, 2nd ed., 2012, ISBN-13: 978-0123944245, ISBN-10: 0123944244; 3. J. Wakerly, Digital Design: principles and practices with Verilog, 5th ed., 2017, ISBN-13: 978-0134460093, ISBN- 10: 013446009X.