

# **ESE 366: Design using Programmable Mixed-Signal Systems-on-Chip**

## **Fall 2020**

**Instructor:** Dr. Alex Doboli.

**Credits:** 4 credits

**Schedule:** TBD.

**Description:** The course presents state-of-the-art concepts and techniques for design of embedded systems consisting of analog, hardware and software components. Discussed topics include system modeling and specification, architectures for embedded mixed-signal systems, performance evaluation, and system optimization. The course follows the top-down design paradigm based on IP cores. Course requirements include three reports on system specification and various co-design tasks.

**Interaction:** The instructor will lecture using a videoconferencing system, like zoom. Office hours will be conducted synchronously using the same system. Lab activities will be carried out synchronously using the videoconferencing system.

**Goal:** Upon completion of the course, students will possess knowledge about state-of-the-art methodologies and techniques for hardware/software co-design of embedded systems. They will be able to (1) develop system-level specifications using high-level languages, (2) model system performance, and (3) implement algorithms for co-design.

### **Text Book and other Teaching Material:**

1. A. Doboli, E. Currie, “Introduction to Mixed-Signal Embedded Design”, Springer, 2010.

### **Covered Topics:**

#### **1) Introduction to Co-Design:**

- a. Problem description, goals of co-design, co-design steps, existing co-design approaches, and present challenges.

#### **2) System Modeling and Specification:**

- a. Models of computation (Signal flow graphs, Data flow model, Task graphs, Finite State Machines, hierarchical models).

#### **3) Architectures for Embedded Systems:**

- a. Single processor – coprocessor architecture, mixed-signal architectures, multiprocessor architectures, reconfigurable architectures, Systems on Chip.

#### **4) Performance Modeling:**

- a. System-level performance modeling vs. low-level performance modeling.
- b. Modeling of system latency, energy consumption etc for hardware and software.
- c. Modeling of analog and mixed-signal systems.
- d. Estimation of memory requirements.

#### **5) System-Level Synthesis and Trade-off Analysis:**

- a. Design of customized digital and analog blocks.

- b. Hardware/software partitioning. Task binding.
- c. IP core integration and communication synthesis: Hardware and software interface synthesis.
- d. Hardware IP core synthesis: High-level synthesis: behavioral specification of hardware, module set allocation, resource binding, operation scheduling, controller design.

**Other Course Material:**

- 1) Other relevant papers will be provided in class.

**Grading:**

$$\text{Final grade} = 0.25 \text{ Lab} + 0.25 \text{ Project} + 0.25 \text{ Midterm} + 0.25 \text{ Final}$$

**Academic Integrity Measures:** Exams will be scheduled face-to-face on campus, if possible. Otherwise, exams will be carried out using a videoconferencing system, like zoom. Also, a significant part of the grade is based on course projects.

**Americans with Disabilities Act/ Student Accessibility Support Center Statement:**

If you have a physical, psychological, medical or learning disability that may impact your course work, please contact Student Accessibility Support Center, ECC (Educational Communications Center) Building, Room 128, (631) 632-6748. They will determine with you what accommodations, if any, are necessary and appropriate. All information and documentation is confidential.

Students who require assistance during emergency evacuation are encouraged to discuss their needs with their professors and Student Accessibility Support Center. For procedures and information go to the following website: <http://www.stonybrook.edu/ehs/fire/disabilities>.

**Academic Integrity:** Each student must pursue his or her academic goals honestly and be personally accountable for all submitted work. Representing another person's work as your own is always wrong. Faculty is required to report any suspected instances of academic dishonesty to the Academic Judiciary. Faculty in the Health Sciences Center (School of Health Technology & Management, Nursing, Social Welfare, Dental Medicine) and School of Medicine are required to follow their school-specific procedures. For more comprehensive information on academic integrity, including categories of academic dishonesty please refer to the academic judiciary website at:

[http://www.stonybrook.edu/commcms/academic\\_integrity/](http://www.stonybrook.edu/commcms/academic_integrity/)